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Technique of High-Field Electron Injection for Wafer-Level Testing of Gate Dielectrics of MIS Devices

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Abstract: We propose a technique for the wafer-level testing of the gate dielectrics of metal–insulator–semiconductor (MIS) devices by the high-field injection of electrons into the dielectric using a mode of increasing injection current density up to a set level. This method provides the capability to control a change in the charge state of the gate dielectric during all the testing. The proposed technique makes it possible to assess the integrity of the thin dielectric and at the same time to control the charge effects of its degradation. The method in particular can be used for manufacturing processes to control integrated circuits (ICs) based on MIS structures. In the paper, we propose an advanced algorithm of the Bounded J-Ramp testing of the gate dielectric and receive its approval when monitoring the quality of the gate dielectrics of production-manufactured MIS devices. We found that the maximum value of positive charge obtained when tested by the proposed method was a value close to that obtained when the charge was injected into the dielectric under a constant current with a Bounded J value despite large differences in the rate of degradation of the dielectric.

Keywords: MIS device; gate dielectric; wafer-level testing; high-field; electron injection; time depend dielectric breakdown

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1. Introduction

Currently, to assess the integrity of the thin dielectric, its defectiveness [1–7], and improve the quality of the technological processes for manufacturing thin dielectrics of MIS structures, methods of Time Depend Dielectric Breakdown (TDDB) are widely used [8–23]. The TDDB methods used for studying and monitoring the production process are regulated by the JEDEC (Joint Electron Device Engineering Council) standards [3,8,14]. One of the most informative methods, suggested by the JEDEC standards, is the Bounded J-Ramp method, which involves increasing the high-field injection current to a specified value (J_{bound}) and maintaining this value until sample breakdown. One of the main disadvantages of this method is the difficulty in tracking the change in the state of the charge as the current increases. Therefore, improving this method, aimed at expanding its functionality by monitoring the charge effects in the gate dielectric, is an important task when studying the degradation processes of an MIS device leading to its failure.

When implementing TDDB to control a change in the charge state of the gate dielectric and its interface with silicon, the C–V technique is widely used [8–10]. However, the use of the capacitance–voltage (C–V) method involves the re-switching of the samples, which can lead to the relaxation of part of the charge accumulated in the gate dielectric in strong fields and, in addition, to the presence of significant inaccuracy in estimating the charge state of the dielectric [24].

The combined use of the TDDB and C–V methods significantly increases the test time, which is highly undesirable when conducting the wafer-level gate dielectric testing of MIS devices in production environments. Thus, the development of new methods and improving the existing ones in order to expand their functionality and increase the

information content while maintaining the control efficiency represent an important and urgent task both from the point of view of monitoring the quality of the gate dielectric and the quality of the gate dielectric production processes of MIS devices.

TDDB techniques are mainly aimed at monitoring the defectiveness of the dielectric film, which correlates with external and internal defects [8–12,25,26]. The formation of external defects mainly correlates with the manufacturing quality (containments, mechanical stresses, vacancies, etc.). The formation of internal defects is mainly determined by the effects caused by the injection of electrons in a strong field and the thermalization of hot electrons (capture of charge carriers by traps in the dielectric, generation of surface states, generation of holes, hydrogen evolution, etc.) [8–11,27–30]. Supplementing the TDDB results with information on the changes in the charge state of the gate dielectric of each sample under study makes it possible not only to determine the quantitative indicators of defectiveness but also to analyze the nature of the formation of defects and develop algorithms for adjusting the technology for forming the gate dielectric to reduce the defectiveness and increase the resistance to strong fields and radiation effects [8,16,17,31–33].

One of the main effects taking place under the TDDB and high-field influences/radiation is a charge accumulation in the gate dielectric of an MIS device [34–41]. The accumulation of charge results in an excessive shift in the threshold voltage and, as a consequence, in an MIS device or IC failure [8–11]. Thus, the device failure, caused by the charge accumulation in the gate dielectric, occurs much earlier than the dielectric film breakdown. Therefore, the change control of the charge state of the gate dielectrics of MIS devices under TDDB improves the manufacturing process of the formation of the gate dielectric, and, as a consequence, increases the device resistance to high-field influences, radiation, and other stress influences.

This paper describes a novel technique for the wafer-level testing of the gate dielectrics of MIS devices by means of the high-field injection of electrons into the dielectrics in the mode of increasing the injection current up to a set level. This technique provides the capability to study the processes of charge state change that result in the failure of the corresponding devices.

The rest of this paper is organized as follows. Section 2 presents the proposed technique of high-field electron injection to test the gate dielectrics of MIS devices. Section 3 describes the experimental sample description, the manufacturing process of the samples, and the experimental equipment. Section 4 presents the experimental results and the discussion of them. Finally, Section 5 consists of the conclusions.

2. Technique of High-Field Electron Injection into the Gate Dielectrics of MIS Structures

For the Bounded J-Ramp at the initial stage, the density of the injection current increases progressively by an exponential law over curtain time periods, which is the same for the J-Ramp, until it reaches a set constant value J_{bound}. This value then remains constant until the sample breakdown [13,15,18–20]. For the Bounded J-Ramp, a change in the charge state of the gate dielectric can be evaluated by the time dependence of the voltage across the MIS structure measured during the test. However, as the current density increases progressively, the injection conditions and magnitude of the electric field are changed at each stage. These changes greatly complicate the analysis of the time dependence of the voltage and thus evaluating the charge characteristics of the gate dielectric being tested.

In order to eliminate this issue and enhance the functional capabilities of the Bounded J-Ramp, this paper proposes an improved test methodology, the algorithm of which is presented in Figure 1.

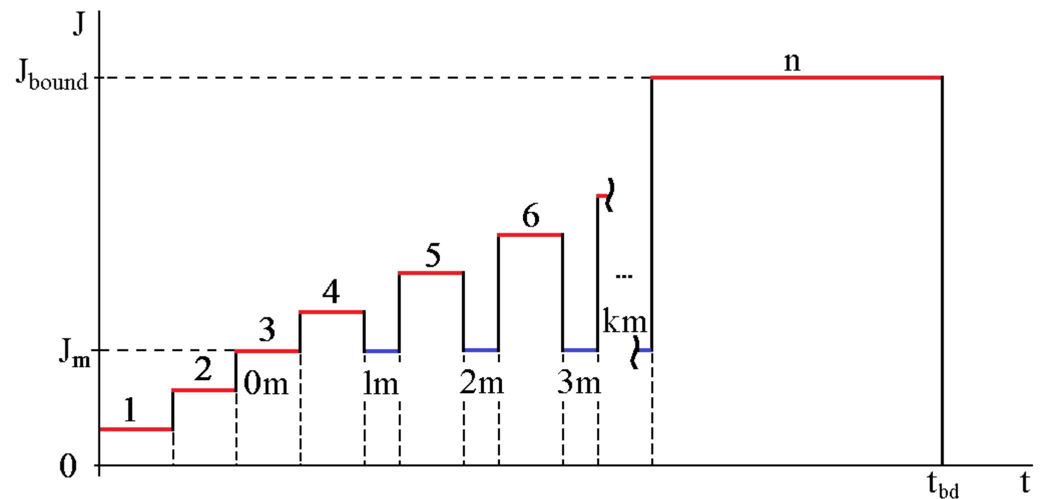

Figure 1. Time dependence values of injection current flowing through the studied MIS structure: 1, 2, 3, 4, 5, 6. . . *n*—stages corresponding to flow of stress injection current; 0 m, 1 m, 2 m, 3 m,. . . km—stages corresponding to flow of measurement injection current.

Figure 1 demonstrates that, for the suggested method, the stress by increasing the current is implemented at stages 1, 2, 3, 4, 5, 6. . . *n*. At the same time, at *n* stage, the stress is implemented with a constant current amplitude of J_{bound}. For the proposed method, at the densities of the injection current at which a change in the charge state of the MIS structure takes place, e.g., Figure 1, stage 4 (this stage is defined by preliminary studies), before the switch to the next step, a short-time switch to injection by the measurement current amplitude J_{m} is implemented (stages 1 m, 2 m, 3 m. . .km).

We set the voltage amplitude $V_{0\text{m}}$ at stage 3 in Figure 1 as the reference value and, regarding it, we evaluate a change in the voltage across the MIS structure after each step of stress by monitoring the voltage at the subsequent measurement stages ($V_{1\text{m}}$,$V_{2\text{m}}$,$V_{3\text{m}}$. . .V_{km}). As a result, we have a shift in the voltage characterizing a change in the charge state of the gate dielectric after each step of current stress influence.

An important difference in the proposed technique in comparison with the regular Bounded J-Ramp is the ability to control a change in the charge state of the gate dielectric when implementing TDDB [13,14]. In comparison with our previously discussed methods based on Bounded J-Ramp [13,14], the paper proposes a novel algorithm of injection current control, which is presented in Figure 1. The use of this algorithm minimizes the quantity of the measurement stages, thus simplifying the test procedure. As a result, the proposed technique could be easily integrated into the manufacturing process to test the gate dielectrics of MIS devices.

Monitoring a change in the charge state of the gate dielectric during the whole test provides the capability to analyze the main physical processes causing the degradation and subsequent breakdown of the gate dielectric.

3. Experimental Samples and Equipment

In order to control defectiveness and study the irreversible degradation processes taking place in the gate dielectric, we use MIS capacitors manufactured in situ with a production batch of MIS devices. This manufacturing process is used to form many discrete MIS transistors and digital ICs of MC74HC series. The MIS capacitors were fabricated on n-type silicon wafers with resistivity of 4.5 Ω·cm and crystal orientation of <100>. The gate dielectric is a silicon dioxide with thickness of 60 nm fabricated by thermal oxidation of silicon in dry oxygen at temperature of 1000 °C mixed with 3% HCl. Then, the wafers are annealed in nitrogen at temperature of 1000 °C. For the gates, we use polysilicon (Si*) films, doped with phosphorus up to 20/square, with thickness of 0.6 µm with 10^{-2} cm^2 area [15,19].

In order to implement the suggested method, we design a test setup based on precise generator/meter of current/voltage PXIe-4135, which is a PXI module from National Instruments. The control application to realize the proposed test algorithm and to monitor the parameters is coded using NI LabVIEW [15–20]. We conduct the studies at positive polarity of the stress, applied to the MIS structure gate, and this enables the electron injection from the silicon wafer and the creation of accumulation mode at semiconductor surface area [15,17,18]. To evaluate a change in the charge state of MIS structure, we also use high-frequency C–V curves.

4. Experimental Results and Discussion

When applying the suggested method to study the charge degradation processes of the gate dielectric, the chosen value of current density J_{bound} has great significance. Figure 2 shows the experimental results demonstrating a change in the charge state of the MIS structures under different densities of the constant injection current. The constant current stress (CCS) technique was used to study in detail the effects of changing the charge state of the gate dielectric at different injection current densities. The CCS was used in order to properly choose the J_{bound} value. A change in the voltage across the MIS structure under high-field electron injection from silicon when in a mode of constant current maintenance characterizes a change in the charge state of the gate dielectric [8,15,17,23,24,42,43]. Figure 2 shows the experimental data for samples with maximum values of charge injected until the breakdown. The gate dielectric breakdown for these samples is caused by presence of internal defects, the evaluation of which under high-field injection results in the gradual formation of a conductive channel in the gate dielectric and its subsequent breakdown [8–11]. Figure 2a demonstrates that, at the initial stage of injection, the accumulation of a positive charge is the main effect causing the degradation of the gate dielectric. The value of the positive charge has field dependence and, consequently, increases with the increase in the density of the injection current (Figure 2). At values of the injected charge in a range of 1–3 mC/cm^2, we can observe a saturation of the positive charge density. Simultaneously, the accumulation of the negative charge in the gate dielectric becomes the main process characterizing the charge degradation of the dielectric.

The accumulation of a negative charge is correlated with the capture of electrons in the bulk of the gate dielectric on the initially existent and newly generated electron traps [8,27–30]. This effect corresponds to a positive voltage increase across the MIS structure (Figure 2a,b). Obtained from Figure 2, the experimental results are in good qualitative agreement with the results of other researchers that were obtained for similar MIS structures [27,30,42,43].

We have determined that, in the gate dielectric, the density of the fast surface states at the Si/SiO_2 interface has begun to increase ten times simultaneously with the generation of the positive charge. In the spectrum of the density of fast surface states, as for [8,27–30], there are two peaks in the bottom and middle parts of bandgap. The main differences in the charge degradation of the gate dielectric at different densities of injection current are the rate of capture and saturation density of the positive charge accumulated in the SiO_2 film. We found that, with an increasing value of the positive charge, a decrease in the mean value of the charge injected until the breakdown occurs. This result is in good agreement with the breakdown model suggested in [8,29,43]. According to that model, all across the MIS capacitor, there are a few “weak spots”, which are capable of capturing an abnormally high amount of the positive charge. At that rate, the areas of “weak spots” to the overall capacitor area is 10^{-7}–10^{-6} [8]. Because the accumulation of a positive charge results in lowering the potential barrier value at the injecting interface, the presence of “weak spots” could lead to a large increase in the local injection currents. Thus, these currents generate a higher positive charge. As a result, in the area of the “weak spot”, positive feedback is created, which leads to structure breakdown [8,43].

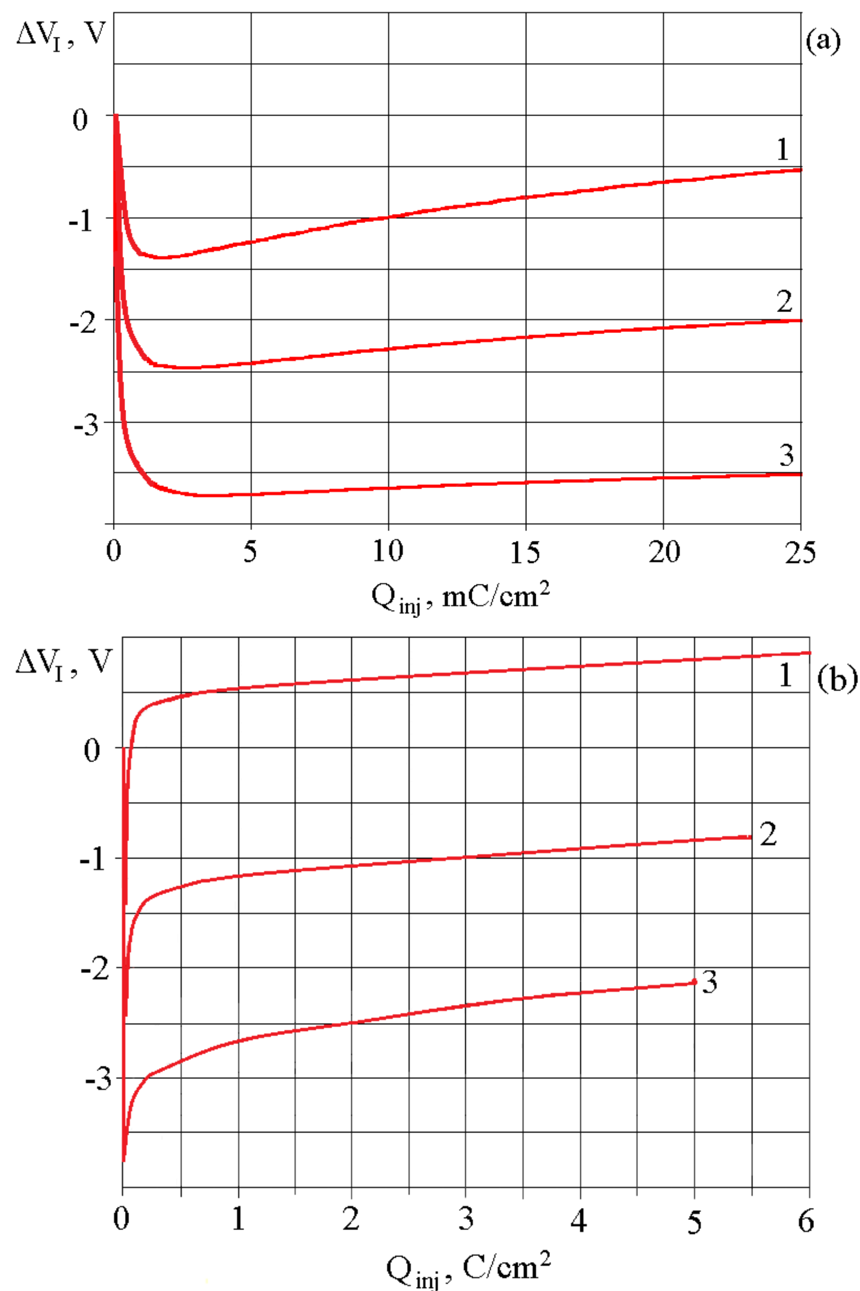

Figure 2. Changes in voltage across MIS structure under high-field electron injection from silicon wafer at initial (**a**) and at overall (**b**) stages of test in the mode of maintaining constant current densities of 1—10^{-4} A/cm^2, 2—10^{-3} A/cm^2, and 3—10^{-2} A/cm^2.

Thus, at low densities of injection current, the rate of generation of the positive charge is relatively low and only the presence of a "rough defect" at the Si/SiO_2 interface or in the SiO_2 film could result in early structure breakdown. With the increase in the density of the injection current, increased defects could cause a local increase in the current density, which leads to the breakdown. Hence, at increased current density, the amount of structures for which the breakdown at low values of injected charge is observed rises. This result could be explained in accordance with the breakdown model suggested in [8,29,43].

According to this model, the injection degradation of the gate dielectric and the Si/SiO_2 interface caused by hot electrons also have irregular distributions across the structure.

The main processes of the charge degradation of MIS structures with dielectric films of the thickness of interest are as follows: the inter-band impact ionization in the SiO_2 film,

which is caused by the "tail" of distribution of hot electrons, resulting in the generation of an electron–hole pair with the subsequent drift and capture of the holes in the dielectric at its interface with silicon; the injection of the holes from the anode; the drift of the holes and their accumulation at the Si/SiO_2 interface; the generation of the surface states, which are created upon the recombination of the captured holes with the injected electrons, and a hydrogen redistribution as a result; and the formation of new electron traps in the SiO_2 bulk, which are created due to the interaction of hot electrons with hydrogen-containing defects. As a result of the injection degradation, an increase in the density of the surface states and accumulation of a positive charge in the SiO_2 film at the Si/SiO_2 interface occur. The irregular distribution of these states across the structure could result in a local rise in the injection current, the subsequent formation of positive feedback, and, as a consequence, structural breakdown. Consequently, the amount of charge injected into the gate dielectric before its breakdown is determined by the injection degradation rate, which increases with increasing electric field. Thus, a lower amount of the charge injected until the breakdown when increasing the density of the constant injection current correlates with increasing the rate of charge degradation of MIS structures.

Accordingly, when controlling the injection stability of MIS structures, it is necessary to take into consideration that the density of the injection current greatly influences the type of revealed defects of charge stability. Increasing the injection current density, on the one hand, increases the efficiency of control. Conversely, it results in the hardening of the test modes and an increase in the amount of structures that are under breakdown at the early stage of injection. Moreover, it results in lowering the mean value of charge injected until the breakdown.

According to the fact that, for most MIS structures with no rough defects, the breakdown of the gate dielectric is defined by a value of the injected charge [8,12,13,15], the value of J_{bound} should be chosen under the condition of the efficient statistical monitoring of a value of the charge injected until the breakdown (Q_{bd}). At low values of J_{bound}, we will have a longer measurement time. Simultaneously, at greater values of J_{bound}, our method becomes mostly the same as the J-Ramp technique [13,18,19].

In Figure 1 at step n, when the current density is limited by the J_{bound} value, generally, there is no necessity to use the measurement levels and switch the current to the J_m value. A change in the charge state at this step can be monitored by a change in the voltage across the MIS structure (ΔV_I), concatenating it with the ΔV_m obtained at the measurement steps (Figure 1). This concatenation becomes possible because of the low dynamics of change in the charge state of the gate dielectric (Figure 2) when changing from the rising current step to J_{bound} (Figure 1).

Figure 3 shows the change in the voltage across the MIS structure under the high-field electron injection in the mode of maintaining a constant current density of 10^{-2} A/cm^2 (curve 1) and when measuring by the proposed method at $J_{bound} = 10^{-2}$ A/cm^2 (curve 2). Figure 3 demonstrates that the maximum value of positive charge, generated in the gate dielectric, is similar for both of the methods considered. When studying the proposed method, the maximum value of the positive charge is reached at greater values of the injected charge, which is caused by the presence of a step with increasing current at which the formation of the positive charge has a significantly lower intensity.

Thus, the results presented in this paper describe a change in the charge state of the gate dielectric on the basis of the measurement of ΔV_m at the step of increasing current and ΔV_I at the step of maintaining the J_{bound} constant current. Those results are almost identical to the results obtained on the basis of the ΔV_m measurement during the whole test. In addition, we have established that the maximum value of the positive charge formed in the gate dielectric when tested by the method presented in the article was similar to the value obtained when the charge was injected into the dielectric in the mode of maintaining a constant current of the same value as the J_{bound}.

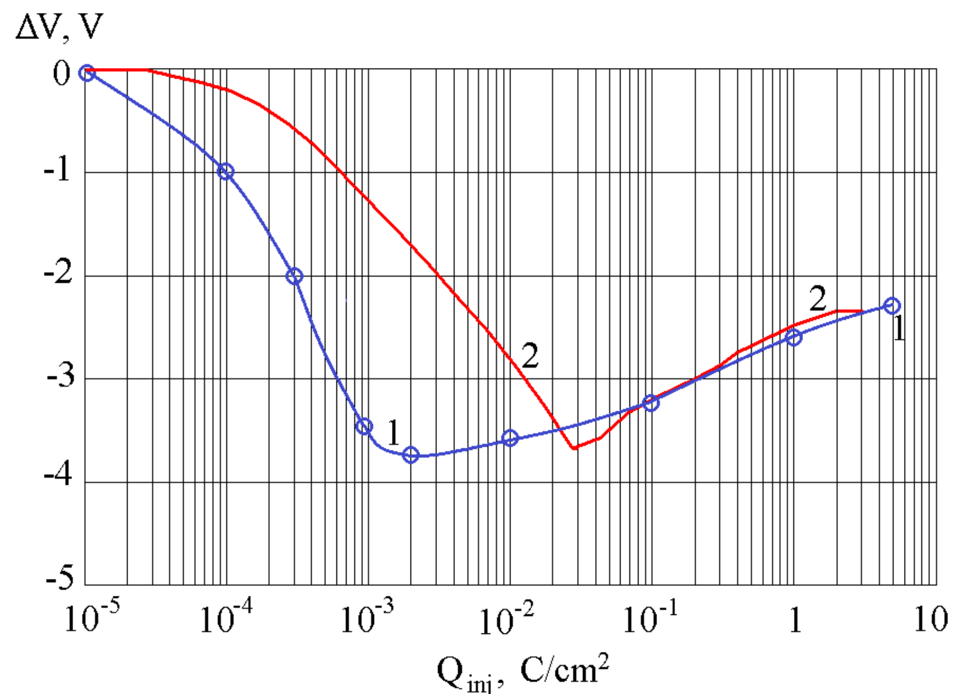

Figure 3. Dependence values of changes in voltage across MIS structure on value of the injected charge under high-field electron injection from the silicon substrate when in the mode of maintaining constant current density 10^{-2} A/cm^2 (curve 1) and when measuring by the presented method at $J_{bound} = 10^{-2}$ A/cm^2 (curve 2).

Monitoring both the defectiveness of the dielectric film and the change in its charge state using the proposed technique was implemented on one hundred test MIS capacitors formed on one semiconductor wafer in accordance with the technological process described above. In order to analyze the statistical distribution of the defectiveness, we use a Weibull plot. This plot characterizes the probability of the gate dielectric breakdown under a set value of charge injected until the breakdown. A Weibull distribution has a bimodal character, which is a superposition of two distribution plots, one of which correlates with the presence of the external defects and the second correlates with the presence of the internal defects [8,12,13,21–23]. A difference in these distributions was observed at a value of about 1 C/cm^2 of the injected charge. More than 65% of the studied samples yielded breakdowns at values of Q_{bd} higher than 1 C/cm^2 and were characterized by internal defects. For all the samples with internal defects, a change in the charge state of the gate dielectric during all the performed tests demonstrated results similar to the data shown in Figures 1 and 2.

Two of the one-hundred studied MIS capacitors have higher changes in the charge state of the gate dielectric in comparison with the results presented in Figures 1 and 2. The breakdown of these capacitors happened at the initial stage of testing. Apparently, the capacitors have rough external defects that correlate with the presence of impurities or structural defects. For the remaining 35% of the MIS capacitors, with external defects and experiencing the breakdown at injected charge values up to 1 C/cm^2, the change in the dielectric charge state remained mainly close to the experimental data shown in Figures 1 and 2, with the only difference being the earlier breakdown of the dielectric. This result is well-explained by the previously discussed models, in accordance with which the area of the external defect is many times smaller than the area of the MIS capacitor, and the local change in the charge state in the defect spot has a small effect on the overall change in the charge state of the sample under study.

Thus, monitoring the changes in the charge state of MIS capacitors, implemented by the proposed TDDB control technique, first of all makes it possible to analyze the

external defects in the gate dielectric. Moreover, this is especially true when the quality of the gate dielectric manufacturing process is low. For many MIS devices, a failure due to the deterioration of the gate dielectric charge occurs much earlier than a failure due to breakdown. Thus, the proposed technique makes it possible to control the test samples not only by the charge injected into the gate dielectric before the breakdown but also by the charge value at which irreversible degradation of the dielectric charge state (Q_{deg}) occurs [15]. A value of Q_{deg} should be selected based on the additional research and testing of MIS devices with a modified gate dielectric.

5. Conclusions

This paper proposes a new technique for testing the gate dielectrics of MIS devices at the wafer level by injecting electrons into the dielectric in a strong field while increasing the injection current to a given level. This method is characterized by a short-term switch to the amplitude of the measuring current after each step of the voltage current. These switches occur at current stress densities that cause a significant change in the charge state of the MIS structure. Voltage monitoring at the measurement stages makes it possible to evaluate a change in the charge state of the dielectric films of MIS structures throughout the test and, on its basis, to study the processes of the charge degradation of the gate dielectric leading to a device failure and the subsequent breakdown of the dielectric film. It was found that a maximum value of positive charge, obtained when testing by the proposed method, had a value close to that obtained when the charge was injected into the dielectric under the influence of a direct current with a value of J_{bound}.

Author Contributions: D.V.A., A.I.P., V.V.A. and M.K. initiated the project. D.V.A. and V.V.A. obtained most of the experimental results and implemented the modeling. A.I.P. coordinated the project and provided access to most of the experimental equipment. The manuscript was written by all the authors. All authors have read and agreed to the published version of the manuscript.

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