Article

The Compact Model Synthesis for the RADFET Device

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Abstract

This article proposes a compact model for the radiation-sensitive field-effect transistor (RADFET). The model represents the basic I–V characteristics of the MOSFET device and includes the effects of threshold voltage shift as a function of absorbed dose and gate bias, gate tunneling current, gate radiation current, dose accumulation, and fading. It accurately represents high-field effects in the gate dielectric of the RADFET device. Both the Fowler–Nordheim gate tunneling current and the radiation-induced gate current are incorporated into the model. The model enables determination of the radiation-induced charge during RADFET operation under high-field injection conditions, thereby improving the precision of accumulated dose readout. The proposed model is fully compatible with SPICE-based circuit simulators and can represent any type of RADFET device, including those with high-k gate dielectrics. Furthermore, the model was developed entirely using open-source circuit simulation tools.

Keywords: MOSFET; RADFET; compact modeling; circuit simulation

1. Introduction

Radiation -sensitive field-effect transistors (RADFETs) are widely used for ionizing radiation monitoring in applications such as aerospace systems, nuclear installations, dosimetry instruments, radiation therapy, and environmental monitoring [1–3]. Typically, p-channel metal-oxide-semiconductor field-effect transistors (PMOSFETs) are employed as RADFET devices. The radiation-induced charge accumulated in the gate dielectric of the MOSFET causes a shift in the threshold voltage V_{t0} [4–6]. By calibrating the dependence of the V_{t0} shift on the accumulated dose, it is possible to determine the absorbed dose from the measured V_{t0} value [1,6,7]. RADFET sensors offer several advantages, including a small active area, low cost, and simple readout circuitry [8,9]. Furthermore, RADFET sensors can be integrated into integrated circuits (ICs) to define the device operating point and enable efficient readout processing [10].

Improving dose sensitivity and utilizing standard CMOS technology nodes such as CD4000 represent key development directions for RADFET sensors [11–13]. Such RADFET sensors typically operate under positive gate bias. This operating mode accelerates the separation of electron-hole pairs generated during device irradiation and increases the radiation-induced charge accumulated in the gate dielectric [14–16]. The dose sensitivity of the RADFET device and the charge work function both increase with the electric field in the gate dielectric. The operation of MOS sensors under high electric fields in the

gate dielectric, particularly under Fowler–Nordheim tunneling conditions, is of special interest [17–19]. The use of high-field electron tunneling enables injection annealing after irradiation [17,19,20]. Our research team has proposed a model describing the charge processes in MOS sensors under various gate biases, extending up to the high-field injection region [21,22]. The proposed model can also describe the annealing process [23,24]. Integrating this mathematical model into SPICE-compatible circuit simulation software would enhance its accessibility. The RADFET SPICE models would be particularly useful for the design of specialized integrated circuits (ICs). Moreover, the SPICE RADFET model could be applied in the design of radiation-hardened ICs, enabling consideration of MOSFET parameter shifts caused by irradiation.

SPICE-based circuit simulation tools [25] are the industrial standard for electronic circuits modelling. The most of proprietary (HSPICE, LTspice) and open source (Ngspice, Xyce) circuit simulation tools are based on original SPICE code developed by L.Nagel. The SPICE simulation kernel supports a set of basic passive and active primitive devices, including resistors, inductors, sources, and transistors. The electronic components not included in a basic set of SPICE devices should be described using macromodels or compact models [26]. The macro model represents a complex device as an equivalent circuit. A compact models differs from a macro model by using only simple devices like controlled sources and RCL components in the equivalent circuit. The electronic components are represented by a set of equations describing the voltages and current at its terminals. There are two ways of compact models integration in circuit simulation software:

1. Using SPICE subcircuits (`.SUBCKT` directive) or macromodels [27]. The compact model is assembled as a set of primitive devices (resistor, capacitor, inductor) and behavioral (B-type) sources representing current on voltage or voltage on current dependencies. This method is supported by every SPICE simulation kernel, but complex models may have a poor performance, because the model parsing is required every time when netlist is loaded.
2. Using Verilog-A hardware description language [28]. The Verilog-A is an extension of Verilog for analog circuits. The Verilog-A models are compiled into binary shared objects that could be attached to the simulator at the execution time. Therefore Verilog-A provides a better performance than subcircuits.
3. Using XSPICE extensions [29,30]. XSPICE modules are written in C programming language with macros and also compiled as shared objects. XSPICE extension are much more difficult to design, but allows to provide a more deep integration of the model and simulation kernel. XSPICE brings no benefit for RADFET model because of design difficulties and no possibility of direct export from schematic. The deep integration with SPICE simulation kernel provided by XSPICE is not required for RADFET device compact model.

In summary, the compact model of the RADFET device can be implemented either as a subcircuit or in Verilog-A form. The Verilog-A implementation is generally preferable, as it offers higher performance. However, since Verilog-A is not supported by some SPICE simulation kernels, such as LTSpice, the subcircuit-based approach provides greater flexibility and broader compatibility.

The RADFET device is not included among the standard SPICE components, which creates a need to develop a custom model. Such a model would enable accurate simulation of the analog part of dosimeter readout circuits using SPICE-compatible circuit simulation tools. The study presented in [31] proposes a modification of the standard SPICE MOSFET model, where the radiation input is represented as a subcircuit parameter. However, this approach has certain limitations, as it employs only a simplified dependence of the MOSFET threshold voltage shift on the absorbed dose. The objective of this research is to extend the model presented in [31] by incorporating additional effects such as gate tunneling current, threshold voltage shift under

irradiation, and fading. These improvements are essential for accurate simulation of analog circuits containing RADFET devices. The work described in [32] introduces a limited compact model of the RADFET device but does not provide implementation details.

The novelty of the presented model, compared to the existing approach based on modifying the SPICE model card, lies in its ability to represent the accumulated dose as a virtual input signal (typically a voltage). This feature is not possible when the dose is introduced as a fixed model card parameter. Consequently, the proposed RADFET compact model enables advanced simulations of circuits that include RADFETs and allows for the estimation of dynamic properties such as fading. In addition, the custom compact model makes it possible to incorporate effects that are not represented in the standard SPICE MOSFET model, which would be difficult to achieve through model card modification alone.

In this article, "radiation" refers to ionizing radiation (for example X-rays, gamma-rays, protons etc.). The sensor and model were calibrated by a gamma-ray source.

The rest of the paper is organized as follows. Section 2 provides an overview of the RADFET device, software used for the model generation, and model equations. Section 3 presents the structure of the generated SPICE model and compares the data from simulation and measurement. Section 4 gives a model usage example for readout circuit design. Finally, Section 5 gives an outcome of the paper and the summary of the achieved results.

2. Materials and Methods

2.1. Used RADFET Device

The RADFET devices [21] were fabricated using the 6 μm CMOS technology compatible with CD4000 logic IC series. The radiation sensor is shown in Figure 1. It consists of two RADFET devices placed in a single ceramic package. Every RADFET is a PMOS device with a channel length of $L = 6$ μm and a channel width of $W = 700$ μm. The n-type silicon wafer doped by phosphorus was used as the substrate. The silicon substrate has 4.5 Ohms per square resistance and <100> orientation. The gate dielectric is silicon dioxide with 100 nm thickness. The total device area is 1,600,000 μm². Micron technology and relatively thick gate dielectric is preferable for RADFET fabrication. The thinner gate dielectric gives the decrease in RADFET sensitivity [33]. The dielectric thickness higher that 100 nm makes sufficient more difficult to implement the Fowler–Nordheim injection mode [34,35].
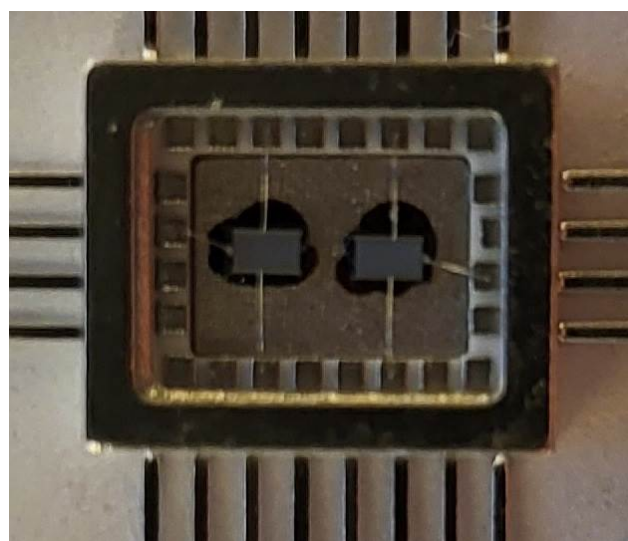

Figure 1. Radiation sensor containing two PMOS RADFET devices.

The layout view of the RADFET device is shown in Figure 2. It uses multi finger topology to achieve large channel width and device area. Every RADFET has three electrodes:

gate, drain and source. The independent gate pin allows to apply gate bias or gate injection current while the device irradiation.
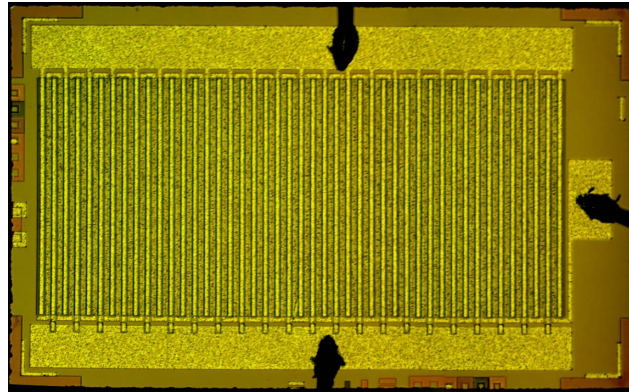

Figure 2. RADFET device layout view.

2.2. Circuit Simulation Software

The Qucs-S circuit simulator (developed by Kuznetsov et al. [36]) was employed for the design of the presented compact model. This open-source tool offers several advantages: it is freely available, provides comprehensive functionality for compact model development, and includes advanced debugging capabilities that support efficient model verification and optimization. It provides access to SPICE directives, parameters, postprocessor directives and equations defined sources, which is needed to construct the compact model. By default Qucs-S uses free Ngspice [37] simulation kernel that is fully compatible with proprietary SPICE tools. There is a possibility to switch to XYCE circuit simulation backend or QucsatorRF backend specialized for RF simulation. Internal Verilog-A synthesizer of Qucs-S allows to export the designed compact model to Verilog-A module. Interactive tuning and optimization tools implemented in Qucs-S graphical user interface (GUI) level allow to perform models parameters extraction. The key feature of Qucs-S is the quick switching between the simulation backends while the program operation. Qucs-S uses external simulation kernel Ngspice [38] and Verilog-A [39] modules compiler OpenVAF. The data flow diagram is shown in Figure 3. It illustrates the interaction between the parts of the simulation software package.
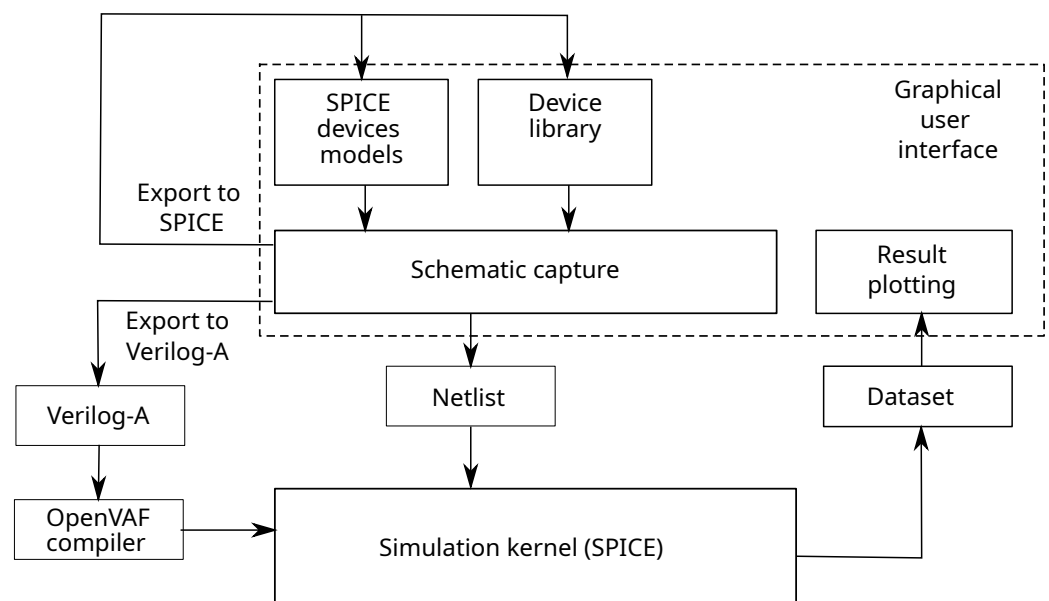

Figure 3. Qucs-S dataflow diagram.

The main application is written using Qt6 framework and operates at the GUI level. The SPICE simulator and OpenVAF Verilog-A compiler are the command line (CLI) application. The communication between the GUI and CLI parts is implemented using the input and output files. The SPICE netlist is automatically generated and saved to file from the schematic view and serves as the input for SPICE backend. The Verilog-A modules could be specified before the simulation. The simulation backend produces a number of dataset files that could be parsed by visualization system of the main application to output graphs representing voltage and current waveforms and frequency domain response of the simulated circuit.

2.3. Basic RADFET Model Equations

All available SPICE simulators provide MOSFET models levels from 1 to 9 and advanced BSIM MOSFET models. The most of RADFET deices are fabricated using the micron technology. And the drain current could be described using MOSFET level 1 equations. MOSFET models levels above 3 and BSIM models [40], which have much more parameters and more complicated extraction procedure, are applicable for submicron devices and have no benefit for RADFET. MOSFET drain current depends on the voltages between the MOSFET pins: gate to source and V_{GS} and drain to source V_{DS}.

The drain current in the linear IV-curve region ($0 \leq V_{DS} \leq V_{GS} - V_{TH}$) is as follows:

$$I_D = \frac{K_p W}{2L} V_{DS}[2(V_{GS} - V_{t0}) - V_{DS}](1 + \lambda V_{DS}), \tag{1}$$

where the V_{t0} is a threshold voltage (V); λ is channel modulation (1/V); and K_p is transconductance (A/V^2);

The drain current in the saturation region, if $0 \leq V_{GS} - V_{t0} \leq V_{DS}$, is

$$I_D = \frac{K_p W}{2L}(V_{GS} - V_{t0})^2(1 + \lambda V_{DS}). \tag{2}$$

The transconductance parameter K_p as the model parameter should be distinguished from small signal transconductance parameter $S = dI_d/dV_g$ expressed in A/V. The source of the RADFET device is internally connected to bulk, and the source-bulk voltage is $V_{SB} = 0$. Therefore, the threshold voltage dependency on bulk potential may not be taken into account.

MOSFET threshold voltage V_{t0} and device transconductance K_p have dependency on the device's absolute temperature T (K) that must be taken into account in the module. The threshold voltage dependency may be approximated by the linear function

$$V_{t0} = V_{t0}(T_{nom}) + TC_{VT0}(T - T_{nom}), \tag{3}$$

where the T_{nom} is the temperature where the initial device parameters could be measured and TC_{VT0} is a temperature coefficient (V/K). The transconductance temperature dependency may be approximated by the power function:

$$K_p(T) = K_p(T_{nom}) \left(\frac{T}{T_{nom}}\right)^\mu, \tag{4}$$

where μ is a coefficient varying in range from 1.3 to 1.5.

2.4. Radiation Dependency of the Threshold Voltage

The threshold voltage shift of the MOSFET can be considered linearly dependent on the absorbed dose D within certain limits. At higher absorbed doses, however, saturation effects become noticeable. The basic model assumes a simple linear dependence of the

threshold voltage shift V_D on the absorbed dose, expressed in rads or grays (Gy), without accounting for saturation effects. In this paper, dose values are expressed in rads:

$$\Delta V_{t0} = SD, \tag{5}$$

where S is a sensitivity coefficient expressed in V/rad. The saturation of the threshold voltage shift at the higher dose may be expressed with a hyperbolic tangent. The more precise approximation proposed in [4,41] may cause convergence issues with SPICE simulator.

$$\Delta V_{t0} = SD_{sat} \tanh(D/D_{sat}), \tag{6}$$

where D_{sat} is a dose at which saturation is reached. Usually $D_{sat} > 10^6$ rad.

The sensitivity has a complex dependency on gate bias during irradiation [42]. This dependency consists of linear and exponential terms:

$$S = S_{lin} - S_{exp} \exp(-V_{gs}/V_b), \tag{7}$$

where the S_{exp} and V_b are the fitting coefficient. If the $S_{exp} = 0$ only the linear dependency on dose is taken into account.

2.5. Gate Current Model

The both MOSFET level 1–9 and BSIM model do not take into account gate current and radiation effects on gate current, which is important for RADFET operation. The gate current I_G could be normalized to gate current density and gate area:

$$I_G = J_G \cdot L \cdot W. \tag{8}$$

The gate current density J_G of the RADFET device consists of three components: capacitive current J_c, high-field tunnel injection current J_{inj}, and radiation current J_{rad}:

$$J_G = J_c + J_{inj} + J_{rad}. \tag{9}$$

Capacitive component J_c could be expressed using the known unity gate capacitance C_{ox} which may be expressed from gate dielectric parameters and gate oxide thickness T_{ox}:

$$J_c = C_{ox} \frac{dV_{GS}}{dt}, \tag{10}$$

$$C_{ox} = \frac{\varepsilon \varepsilon_0}{T_{ox}}, \tag{11}$$

where ε is a gate dielectric (for example, SiO$_2$) permittivity and ε_0 is a dielectric constant. The standard SPICE Level 1–9 MOSFET models used for micron-scale technologies do not provide a parameter for defining the gate dielectric permittivity.

The injection current could be expressed using the Fowler–Nordheim equations:

$$J_{inj} = A\varphi_B^{-1} \left(\frac{V_{GS}}{T_{ox}} \right)^2 \exp\left(-\frac{B\varphi_B^{3/2} T_{ox}}{V_{GS}} \right), \tag{12}$$

where φ_B is a barrier potential (V); $A = 1.54 \cdot 10^{-6}$ A $\cdot$ eV $\cdot$ V^{-2} and $B = 6.83 \cdot 10^9$ eV$^{-3/2}$. V $\cdot$ m^{-1} are Fowler–Nordheim tunneling constants.

The radiation current is expressed by the following Equation [21]:

$$J_{rad} = qY(E)K_g T_{ox} \frac{dD}{dt} \tag{13}$$

where q is the charge of electron, K_g is a value of electron-hole pair per dose unit and SiO$_2$ volume ($8 \cdot 10^{12}$ cm$^{-3} \cdot$ rad^{-1}). The $Y(E)$ is the charge yield under irradiation. The charge yield $Y(E)$ is the fraction of holes that escape initial recombination [15]. This value measured in arbitrary units. It depends on the field E in the gate dielectric. The charge yield could be determined from the data provided by Schwank et al. [15]. We use the following approximation in the compact model:

$$Y(E) = Y_{max} \tanh(E/E_{sat}), \tag{14}$$

where the Y_{max} and E_{sat} are the fitting constants depending on radiation type (gamma-ray, protons, etc.). The plots of the approximation function are shown in Figure 4. It shows good match with experimental plots from [15]. The typical values for Y_{max} and E_{sat} coefficients are given in Table 1.
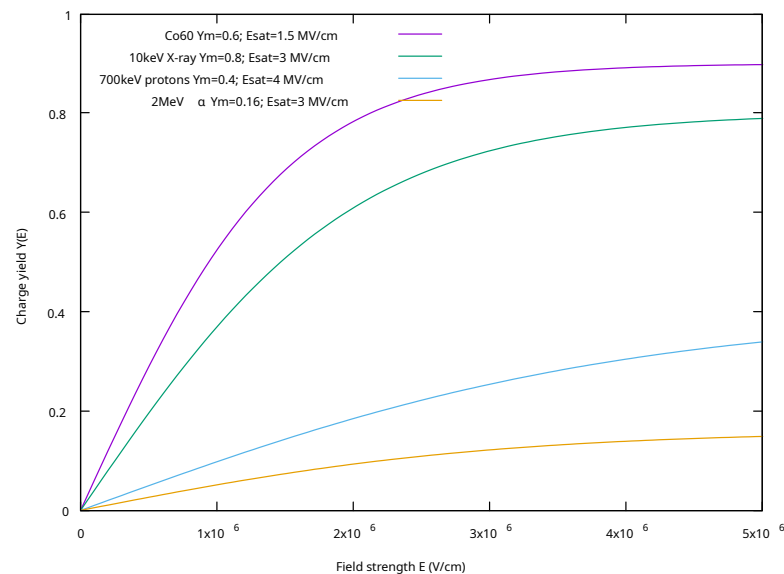

Figure 4. Charge yield approximation.

Table 1. Charge yield approximation coefficients.

Radiation Source	Y_{max}	E_{sat} **(MV/cm)**
Co60 γ-ray	0.6	1.5
10 keV X-ray	0.8	3.0
700 keV protons	0.4	4.0
2 MeV α particles	0.16	3.0

3. Results

3.1. The Equivalent Circuit of the RADFET Device

The compact model represented by the following equivalent circuit designed in Qucs-S is shown in Figures 5 and 6. For convenience of representation the schematic is splitted into two parts. The first part represents the drain current. The second part represents the gate model.
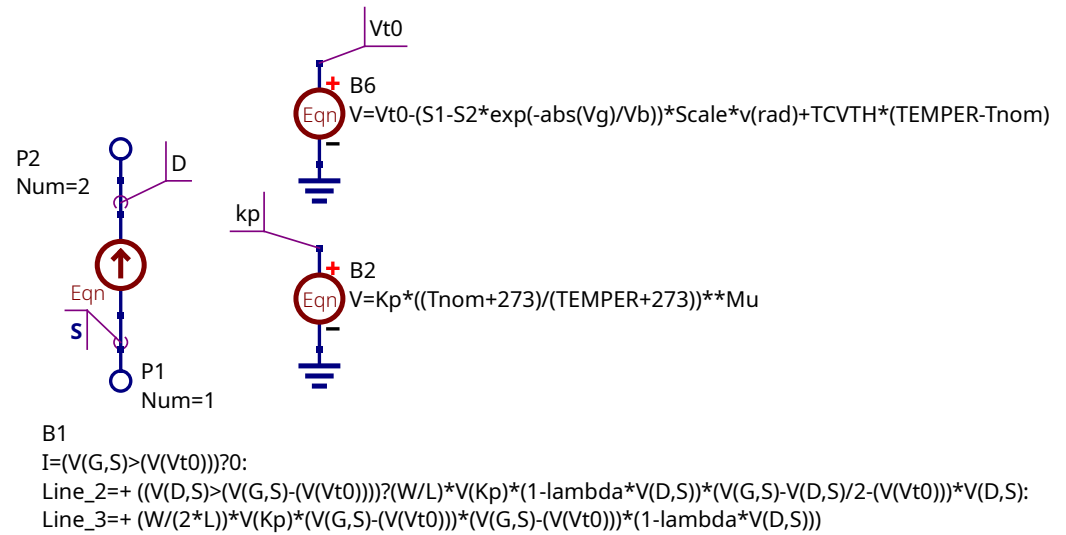
Vt0

+ B6
Eqn V=Vt0-(S1-S2*exp(-abs(Vg)/Vb))*Scale*v(rad)+TCVTH*(TEMPER-Tnom)

–

P2
Num=2

D

kp

+ B2
Eqn V=Kp*((Tnom+273)/(TEMPER+273))**Mu

–

Eqn

S

P1
Num=1

B1
I=(V(G,S)>(V(Vt0)))?0:
Line_2=+ ((V(D,S)>(V(G,S)-(V(Vt0))))?(W/L)*V(Kp)*(1-lambda*V(D,S))*(V(G,S)-V(D,S)/2-(V(Vt0)))*V(D,S):
Line_3=+ (W/(2*L))*V(Kp)*(V(G,S)-(V(Vt0)))*(V(G,S)-(V(Vt0)))*(1-lambda*V(D,S)))

Figure 5. The equivalent circuit representing the RADFET compact model: drain current stage.

P3
Num=3

G

3

Eqn Eqn C1
C=eps*eps0*L*W/Tox

S

Equation
Eqn1
eps0=8.854e-12
eps=3.9
Area=L*W
phiB=3.1
A=1.54e-6 * (1/phiB)
B=6.83e7*(phiB**1.5)*(0.5**0.5)
q=1.6e-19
Ye=0.8
Kg=8e12
ToxCM=Tox*100
AreaCM2=Area*1e4
Esat=1e6
Yem=1.0

B3
I=A*((V(G,S)/ToxCM)**2)*exp(-B/(abs(V(G,S))/ToxCM))*AreaCM2*sgn(V(G,S))

B4
I=q*Kg*ToxCM*(V(DradDt))*AreaCM2*Yem*tanh(abs(V(G,S)/ToxCM/Esat))

RAD P4
Num=4

DradDt

L1
L=1

B5
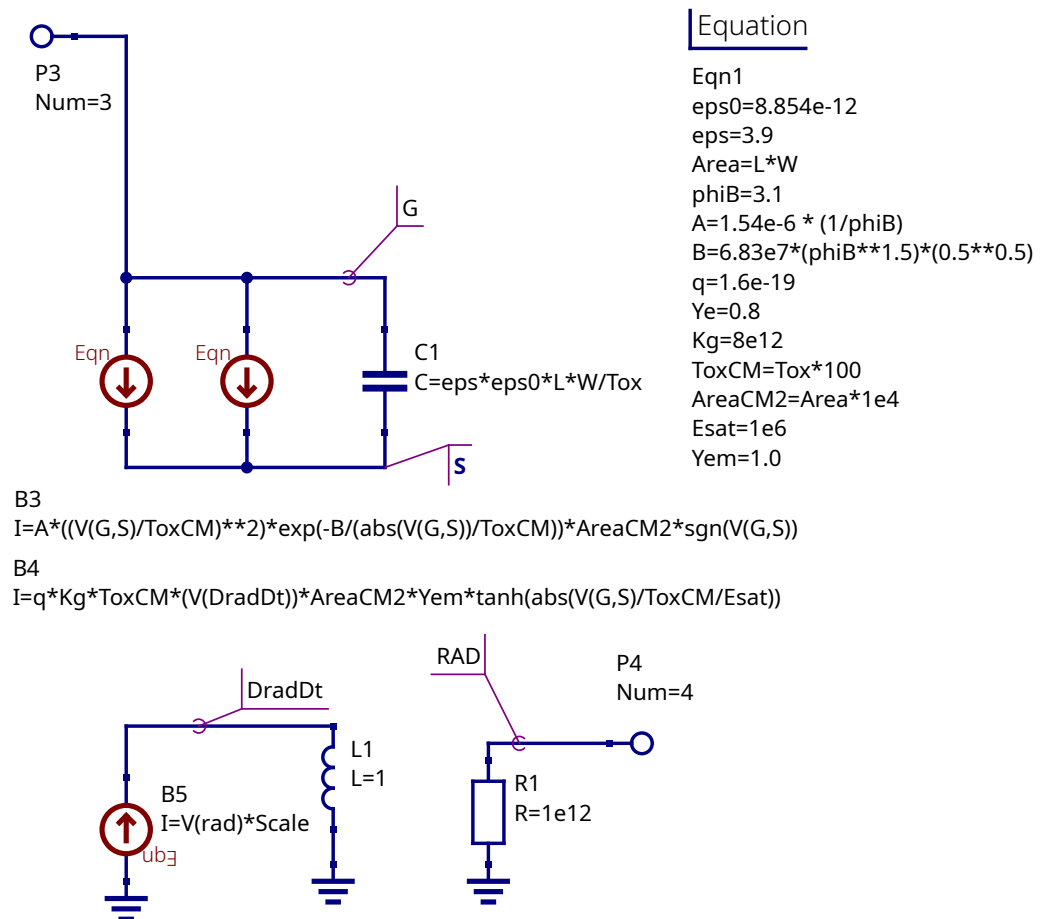I=V(rad)*Scale

R1
R=1e12

Eqn

Figure 6. The equivalent circuit representing the RADFET compact model: gate and radiation input.

The equivalent circuit consists of a number of behavioral current and voltage sources and equation defined passive devices. The model has three terminals for MOSFET electrodes: gate (G—port P3), source (S—port P1), and drain (D—port P2). The fourth terminal (RAD—port P4) serves as the virtual radiation input. The voltage source representing the absorbed dose in rads should be connected to this terminal. The input voltage at the RAD terminal is a virtual signal, and this input is excluded from the operation conditions

check (OCC). The unit scale on this input could be set using the Scale model parameter. Set Scale = 1 for 1 V = 1 rad, or Scale = 1000 for 1 V = 1 krad. The dose D is related to the voltage V_{rad} at the radiation input as follows:

$$D = V_{rad} \cdot Scale. \tag{15}$$

The Equation block in Figure 6 represents the parameters calculated before the simulation using the subcircuit parameters. This block is mapped to `.PARAM` block in the SPICE netlist. The B1 source represents the drain current level 1 MOSFET model with Equations (1) and (2).The transconductance parameter K_p is represented as the virtual voltage. The B2 source is responsible for transconductance temperature dependency (4). The B3 and B4 current sources represent the gate injection (12) and radiation (13) currents respectively. The capacitor C1 is the gate capacitance C_{ox} (11). The L1 inductor and B5 source are a differentiation stage and serve to obtain the radiation intensity dD/dt using the fundamental properties of inductor current. The B6 controlled source represents a threshold voltage shift dependency on the absorbed dose taking into account gate bias. It relates to Equation (7). The equations placed on schematic field are B-type sources component parameters. It's shown how to convert the equations to SPICE notation.

The model parameters are summarized in Table 2. This table provides parameter default value, desciption, and unit.

Table 2. RADFET model parameters.

Model Parameter	Default Value	Unit	Description
V_{t0}	-1.0	V	Threshold voltage at no radiation
K_p	10^{-5}	A/V²	Transconductance coefficient
λ	0.001	1/V	Channel modulation
L	1.0	m	Device length
W	1.0	m	Device width
T_{ox}	10^{-7}	m	Gate dielectric thickness
ε	3.9	–	Gate dielectric relative permittivity
$TCVTH$	1×10^{-3}	V/K	Threshold voltage temperature coefficient
μ	1.5	–	Transconductance temperature coefficient
S_{lin}	0.0015	V/rad	Linear sensitivity component
S_{exp}	0.0	V	Exponential sensitivity
V_b	3.0	V	Exponential sensitivity fitting coefficient
V_g	0.0	V	Gate bias at the irradiation time
D_{sat}	10^7	rad	Saturation dose
T_{nom}	26.85	°C	temperature at which device parameters were measured
$Scale$	1	V/rad	Unit scale for the radiation input

Qucs-S allows to export the schematic representation of the compact model to a SPICE netlist or Verilog-A module. This subcircuit models could be imported by the most of existing SPICE compatible circuit simulation software. The parameters specified in Table 2 are transferred as the subcircuit parameters. Both the SPICE and Verilog-A forms of the compact models could be accessed via the Zenodo link (see the data availability statement in the end of the paper.)

3.2. Equivalent Circuit Representing Dose Accumulation and Fading

The fading [41] shows the decay of the threshold voltage shift after the irradiation:

$$F = \frac{V_{t0}(0) - V_{t0}(T)}{V_T(0) - V_{t0}}, \tag{16}$$

where $V_{t0}(0)$ is the threshold voltage after the irradiation, $V_{t0}(T)$ is the threshold voltage after time T, and V_{t0} is the threshold voltage without irradiation.

The schematic shown in Figures 5 and 6 could be modified to simulate the fading. The dose accumulation and fading could be represented by adding an RC-circuit stage (Figure 7). The time constant of the RC circuit represents the fading time.
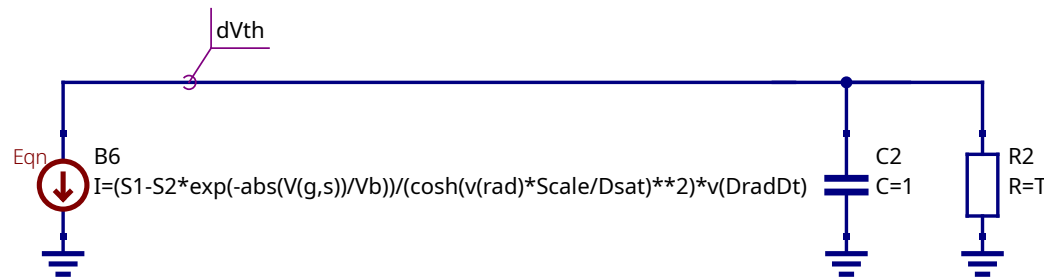

Figure 7. The RC stage representing fading and charge accumulation.

The capacitor C2 is charged from the current source B6 which current I_{charge} is proportional to the time derivative of the threshold voltage shift:

$$I_{charge} = \frac{d\Delta V_{t0}(D)}{dt}. \tag{17}$$

Substitution of (6) and (7) into the (17) yields the equation of the B6 source current:

$$I_{charge} = \frac{S_{lin} - S_{exp}\exp(-V_{gs}/V_b)}{\cosh((D/D_{sat})^2)} \cdot \frac{dD}{dt}. \tag{18}$$

The capacitor voltage is proportional to the integral of the current, and the voltage at the upper capacitor node corresponds to the threshold voltage shift. The discharge of the capacitor through the resistor R2 represents the fading effect. As the capacitor discharges, the threshold voltage shift gradually approaches zero, and the MOSFET threshold voltage returns to its pre-irradiation value.

The part of the compact model representing fading (RC circuit shown in Figure 7) is optional and may be omitted if the fading simulation is not required. Adding the fading stage adds the parameter T_{fad}, representing fading time constant. This additional parameter could be extracted from the threshold voltage shift fading dependency [41].

3.3. IV-Curves Simulation

The V_{t0}, K_p, and λ are the MOSFET level 1 model parameters. Its extraction procedure is well described in the literature and not considered here. The pair of $I_d - V_d$ and $I_d - V_g$ curves are required. The used RADFET device is compatible with the CD4000 technology and these parameters could be taken from the basic technology using common SPICE model extraction methods based on IV-curve properties.

The temperature dependency parameters $TCVTH$ and μ are extracted from fitting of the zero temperature coefficient point at the $I_d - V_g$ curves family at different temperatures within the device operation range. The modeled ZTC point should match the measured ZTC point.

An example of the temperature parameters extraction is shown in Figure 8. The ZTC point for the used device achieved at the drain current $I_d = 10$ μA. The interception points of the IV-curves shown in the figure is located near 10 μA current.
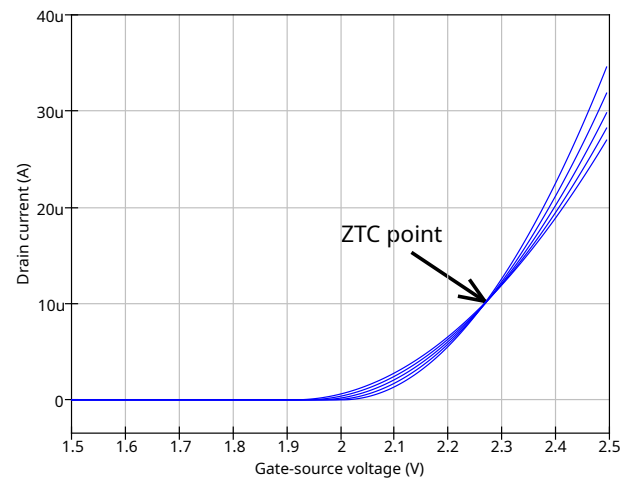
Figure 8. Temperature dependency extraction of RADFET device.

3.4. Sensitivity Simulation

The sensitivity extraction requires the measurement of the I–V curves under different irradiation levels. We have measured the $I_d - V_g$ curves for three irradiation doses: 7 krad, 10 krad and 15 krad with no bias applied at gate. This data was used for sensitivity extraction. The testbench schematic in Qucs-S is shown in Figure 9. The V3 voltage source represents the absorbed dose input. The voltage at this terminal is equal to the dose in rads. Experimental results were obtained using an experimental setup implemented using a PXIe-4135 precision current/voltage generator/meter (National Instruments, Austin, TX, USA) , which is a module of the PXI series from National Instruments. The setup is comprehensively described in [18].
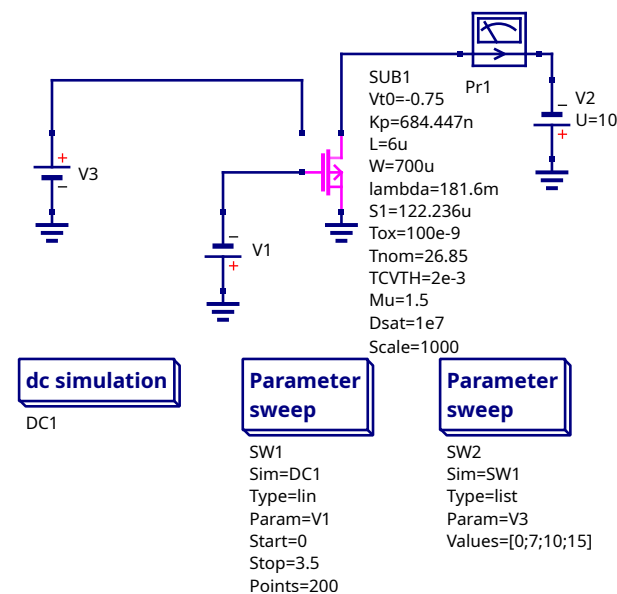
Figure 9. Testbench schematic for I–V curves measurement.

The simulated and measured I–V curves are shown in Figure 10. The figure shows four I–V curves. The measurements were taken without radiation and under radiation levels 7 krad, 10 krad, and 15 krad. The gamma-ray ^{60}Co source was used.
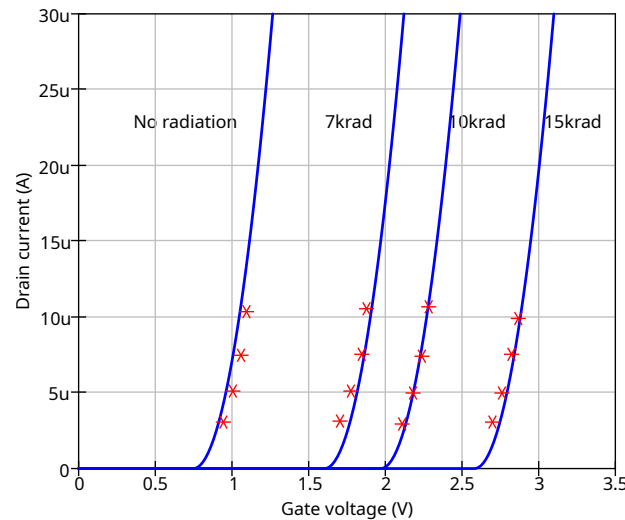
Figure 10. Simulated (solid line) and measured (stars) I–V curves for the RADFET device.

3.5. Gate Bias Dependency of Sensitivity

The sensitivity could be extracted as the derivative of the threshold voltage:

$$S = \frac{d}{dD}(V_{t0} + \Delta V_{t0}(D)). \tag{19}$$

The threshold voltage can be measured by connecting the MOSFET drain and gate to a current source while grounding the source terminal. When the source current is in the microampere range, the voltage at the drain node closely approximates the threshold voltage. The testbench schematic and the sensitivity extraction script are shown in Figure 11. Nutmeg, the scripting language of the Ngspice simulator, is used to assemble a vector representing the $S(V_{bias})$ dependency based on the results of a single-point DC sweep simulation.
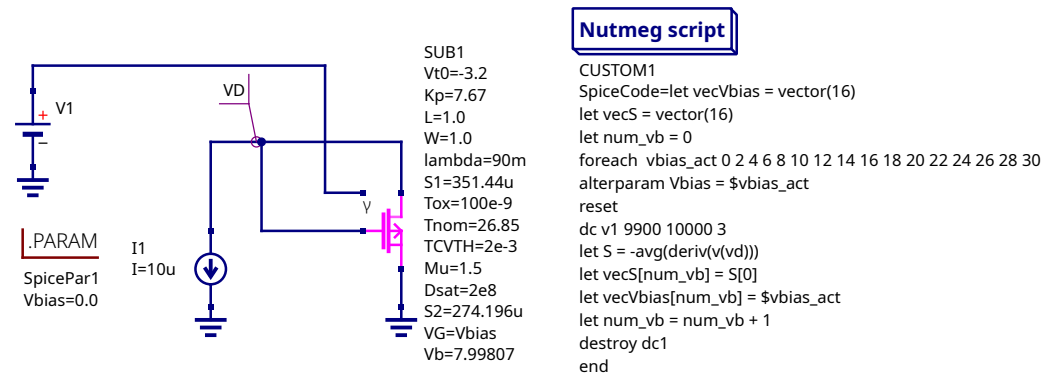

Figure 11. Testbench schematic for sensitivity extraction.

The simulation results are presented in Figure 12. The data for the IRF9520 power MOSFET, provided in [4], were used since the gate bias dependency for the device described in Section 2.1 was not experimentally measured. The parameters K_p, V_{t0}, and λ for this MOSFET were taken from the SPICE VDMOS model supplied by the device vendor. The simulation demonstrates good agreement with the experimental data. The extracted parameters are as follows: $S_{lin} = 0.351$ mV/rad, $S_{exp} = 0.274$ mV, and $V_b = 7.99$ V.
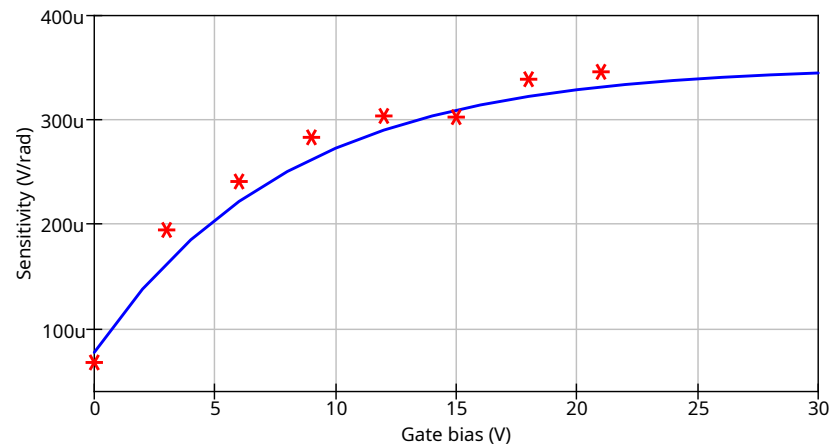
Figure 12. Simulated (solid line) and measured (stars) sensitivity dependency on the gate bias.

3.6. Gate Current Simulation

The study presented in [22] demonstrates that utilizing gate charge injection in RAD-FET devices extends their range of applications. Circuit simulation enables the analysis and debugging of dosimeter circuits that operate with gate injection current. The testbench schematic for gate current simulation is shown in Figure 13. In this setup, a DC injection current source (I1) is connected to the MOSFET gate, while all other terminals are grounded. The pulsed voltage source V1 represents a virtual radiation beam, where the pulse rise time corresponds to the irradiation duration and the peak voltage represents the radiation dose D. During transient simulation, the gate voltage drop at the gate node is monitored. Both the drain and source terminals are connected to ground. The virtual current probe Pr1 is used to measure the gate current.
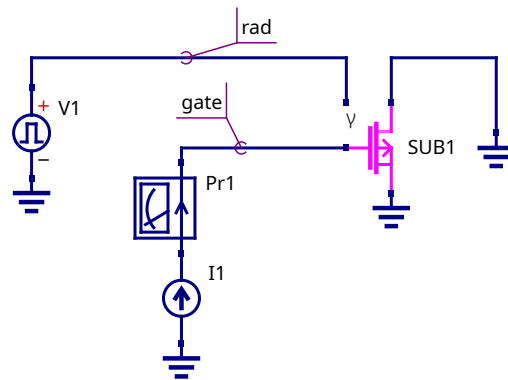

Figure 13. Testbench schematic for the gate current simulation.

Figure 14 shows the simulation result for the testcase described in the paper [22]. The MOS sensor (RADFET) was injected by current density $J_{inj} = 10^{-7}$ A/cm². Then it was irradiated by gamma-rays to achieve the radiation current density higher than injection current density. The voltage drop on the MOS structure (RADFET) depends on the ratio of the radiation current and total current. When the radiation intensity dD/dt increases, as well as the radiation current, but the voltage drops as the gate decreases. The simulation shows a good match with the data provided in [22].
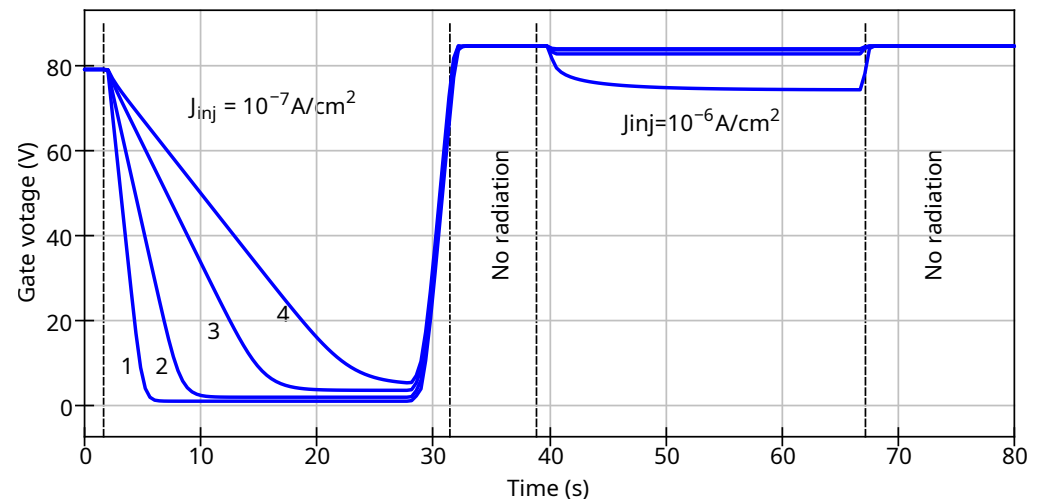
Figure 14. Waveform of the voltage at RADFET gate under injection and irradiation for different ratio of injection and radiation currents. 1—$J_{rad} = 10J_0$; 2—$J_{rad} = 5J_0$; 3—$J_{rad} = 3J_0$; 4—$J_{rad} = 2J_0$.

4. Discussion

In the paper [18], we proposed the design of MOS radiation sensor capable of operating under conditions of high-field injection of electrons into the gate dielectric. Experimental testing of the developed sensors was carried out using gamma radiation, alpha particles and protons. The article proposed a physical model describing the physical effects occurring in the MOS sensor when exposed to ionizing radiation in a wide range of electric fields applied to the dielectric (including high-field electron injection). This article is a continuation of the research presented in [18], and in it, the previously described physical effects are taken into account in the SPICE model. As a result, it becomes possible to design RADFET sensors with specified electrophysical and metrological characteristics at the development stage. Also, depending on the modeling, it becomes possible to create more complex electronic devices for monitoring radiation, in which, along with the RADFET sensor, there are electronic components that improve the metrological characteristics and readout (telemetry) of radiation characteristics.

The designed compact model makes it possible to simulate the input stage of the dosimeter described in [43] along with its analog front end. The dosimeter input schematic is shown in Figure 15. The LM334 current source IC (REF1) provides a constant current to the drain and acts as an adjustable current source, which is commonly used in dosimeter readout circuits. The resistor R1 sets a current of 10 µA, with its selection guidelines available in the IC datasheet. A SPICE macro model for the LM334 IC is supplied by the device vendor. Switches S1 and S2 are used to simulate the irradiation and measurement phases, respectively. The pulsed voltage source V1 represents a virtual radiation input, where its high voltage level U2 corresponds to the total accumulated dose. The 1 V voltage at the radiation input (wire labeled with rad) represents 1 krad dose. The rise time Tr of the pulsed source represents the duration of the irradiation phase. The delay T1, defined as the time between the start of the simulation and the beginning of the pulse, is used to improve the visual clarity of the simulation plots and can be set arbitrarily. The total pulse duration T2 should be longer than the overall simulation time. At the start of the simulation, switch S1 is closed and S2 is open. The states of the switches change at time $T1 + Tr$. During irradiation, all electrodes of the RADFET are connected to ground, and the sensor operates under exposure. When the irradiation phase ends, S1 opens and S2 closes, switching the MOSFET into the measurement circuit. Under these conditions, the drain voltage corresponding to the selected drain current range is approximately equal to the

MOSFET threshold voltage V_{t0}. The virtual current probe Pr1 is used to monitor and verify the DC operating point of the circuit.
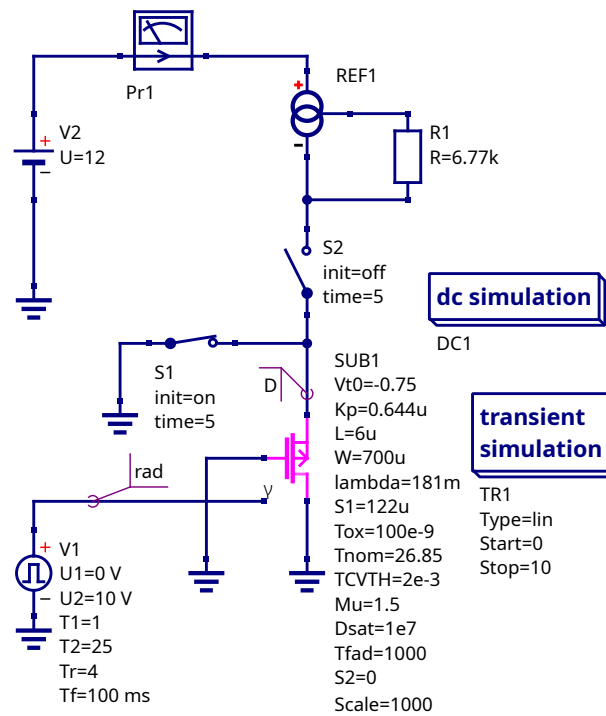

Figure 15. The schematic of the dosimeter input designed in Qucs-S.

The simulated output voltage and input radiation dose are shown in Figure 16. During the irradiation phase, the drain voltage is equal to zero because the RADFET is disconnected from the readout circuit and its terminals are shorted. In the readout phase, the drain voltage is approximately $V_D = V_{t0} + S_{lin}D$, since the applied dose (10 krad) does not approach the saturation region and no gate bias is applied during irradiation.
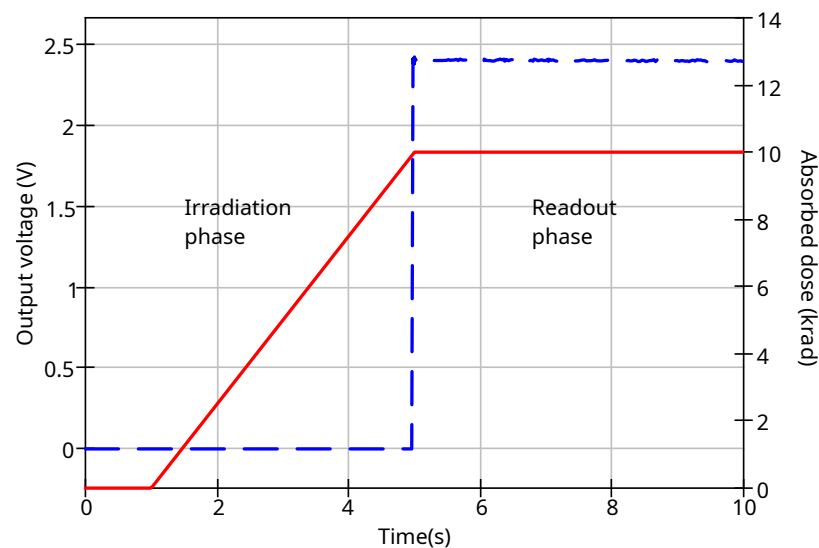

Figure 16. The simulated output voltage of the dosimeter (dashed curve, left Y-axis) and accumulated dose (solid curve, right Y-axis).

The considered schematic shows how to use the presented RADFET compact model for the readout circuits simulation. The fading is not taken into the account. The presented approach could be extended to more complex readout circuits.

5. Conclusions

This paper presented a compact model of the RADFET device. The proposed model offers a more flexible approach compared to substituting the threshold voltage shift dependency on the accumulated dose directly into a SPICE model card parameter. The model features a dedicated input for a virtual radiation source, enabling simulation of the complex behavior of dosimeter input circuitry in response to varying radiation beam dynamics. The developed model extends standard SPICE MOSFET models and allows simulation of the following effects:

- Basic MOSFET IV-curve dependency;
- Threshold voltage shift dependency on the adsorbed does and gate bias at the irradiation phase;
- Saturation at high absorbed dose;
- Gate dielectric properties;
- Tunneling gate current and irradiation gate current;
- Threshold voltage fading after the irradiation.

A limitation of the proposed model is that the charge yield coefficient $Y(E)$ is not calculated automatically and must be manually adjusted for different types of radiation sources (for example, protons). Additionally, the bulk terminal and the threshold voltage dependency on the bulk voltage were omitted since the device's bulk is connected to the source terminal.

The presented model is modular, allowing the fading submodule to be disabled when fading simulation is not required. The model parameters can be extracted from IV-curve measurements and threshold voltage shift measurements obtained during irradiation. The proposed model is fully compatible with the standard Level 1 SPICE MOSFET model and can be used with both open-source and proprietary SPICE simulation kernels. It is implemented in subcircuit form but can be converted to Verilog-A using a Verilog-A synthesizer. The use of the proposed compact model enables accurate simulation of dosimeter analog readout circuits, taking into account both the accumulated dose and the gate bias applied during irradiation. This capability is demonstrated through an example simulation of the dosimeter readout schematic.

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